a second transistor;

reducing the external voltage by a threshold voltage of the transistor by a threshold voltage of both the first transistor and the second transistor; and

providing [a] the reduced voltage at a second source/drain of the second transistor[, wherein the reduced voltage is the external voltage reduced by a threshold voltage of both the first transistor and the second transistor]; and

applying the reduced voltage to the at least one internal circuit.

REMARKS

Claims 22, 27-28, 34, 38, 41, 45, 49, 52, 61, 63, 65, 69, 72, and 75 and no claims are added or canceled; as a result, claims 22-77 remain pending in this application.

The amended claims are not amended in response to any rejection. Moreover, the claim amendments merely clarify the claims and are not believed to be narrowing.

§112 Rejection of the Claims

Claims 22-77 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully traverses.

In rejecting a claim under the second paragraph of 35 USC 112, the examiner must establish that one of ordinary skill in the art, when reading the claims in light of the specification, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims. *Ex parte* Wu, 10 USPQ 2d 2031, 2033 (B.P.A.I. 1989). Applicant believes that a *prima facie* indefiniteness rejection has not been made. For example, interpretation of the claims in view of the specification has not been made. Reconsideration and withdrawal of the §112 rejection is requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-349-9587) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 16 Jan 2003 By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 16th day of January, 2003.

Name Amy Moriarty

Signature

Docket No. 703.019US3
WD # 407096

Micron Ref. No. 97-0445.02

Clean Version of Pending Claims

SUPPLY VOLTAGE REDUCTION CIRCUIT FOR INTEGRATED CIRCUIT
Applicant: Christophe J. Chevallier
Serial No.: 09/955,270

Claims 22-77, as of January 16, 2003 (date of response to first office action filed).

C1 Sub D1

22. (Amended) A method of reducing a voltage, comprising:

applying the voltage to a transistor;

reducing the voltage by a threshold voltage of the transistor; and

providing the voltage reduced by the threshold voltage of the transistor at an output of the transistor, wherein the output of the transistor is coupled to a well that bounds the transistor.

23. The method of claim 22, wherein applying the voltage to the transistor comprises coupling the voltage to a first source/drain and a gate of the transistor.

24. The method of claim 23, further comprising coupling the output of the transistor to a second source/drain of the transistor and to a semiconductor region in which the first and second source/drains are formed.

25. The method of claim 24, wherein the first and second source/drains and the well are formed from a first type semiconductor material and the semiconductor region is formed from a second type semiconductor material.

26. The method of claim 25, wherein the first and second source/drains contain a different dopant concentration relative to the well.

27. (Amended) A method of reducing a voltage, comprising:

applying the voltage to a first source/drain and a gate of a transistor;

reducing the voltage by a threshold voltage of the transistor; and

providing the voltage reduced by the threshold voltage of the transistor at a second source/drain of the transistor and a well bounding the transistor.

28. (Amended) The method of claim 27, further comprising coupling the well that bounds the transistor to the second source/drain of the transistor.

29. The method of claim 28, further comprising coupling a semiconductor region in which the first and second source/drains are formed to the well region and to the second source/drain.

30. A method of reducing a voltage applied to a circuit, comprising:

coupling a transistor between the voltage and the circuit to reduce the voltage by a threshold voltage of the transistor; and

coupling a well, that isolates the transistor from a substrate, to the circuit.

31. The method of claim 30, wherein coupling the transistor between the voltage and the circuit comprises:

coupling one source/drain of the transistor to the voltage;

coupling a gate of the transistor to the voltage; and

coupling another source/drain of the transistor to the circuit.

32. The method of claim 30, wherein coupling the transistor between the voltage and the circuit comprises:

coupling one source/drain of the transistor to the voltage;

coupling a gate of the transistor to the voltage;

coupling another source/drain of the transistor to the circuit; and

coupling a semiconductor region, containing the one source/drain and the other source/drain, to the circuit.

33. The method of claim 32, wherein the one source/drain, the other source/drain and the well are formed from a first type semiconductor material and the semiconductor region containing the one source/drain and the other source/drain is formed from a second type semiconductor material.

Sub D1 C3

34. (Amended) A method of reducing a voltage, comprising:

applying the voltage to a first source/drain and a gate of a transistor;

reducing the voltage by a threshold voltage of the transistor; and

providing the voltage reduced by the threshold voltage of the transistor at a second source/drain of the transistor, wherein a semiconductor region containing the first and second source/drains is coupled to the second source/drain of the transistor.

35. The method of claim 34, further comprising:

isolating the transistor from a substrate by a well formed between the region containing the first and second source/drains and the substrate; and

coupling the well to the second source/drain and to the semiconductor region containing both source/drains.

36. The method of claim 35, wherein the first and second source/drains and the well are a first type semiconductor material and the region containing the source/drains is a second type semiconductor material.

37. The method of claim 36, wherein the first and second source/drains have a different dopant concentration than the well.

38. (Amended) A method of reducing voltage from an external voltage supply in an integrated circuit, comprising:

coupling a transistor of the integrated circuit between the external supply voltage and an internal circuit of the integrated circuit;

reducing the external supply voltage applied to the internal circuit by a threshold voltage of the transistor;

isolating the transistor from a substrate region of the integrated circuit by a well formed in the substrate region; and

coupling the well to the internal circuit.

39. The method of claim 38, wherein coupling the transistor between the external supply voltage and the internal circuit, comprises:

coupling a first source/drain and a gate of the transistor to the external supply voltage; and

coupling a second source/drain of the transistor, the well, and a semiconductor region containing the first and second source/drains of the transistor to the internal circuit.

40. The method of claim 38, wherein the integrated circuit is a memory device and the internal circuit is a memory cell of the memory device.

41. (Amended) A method of reducing voltage, comprising:

applying the voltage to a first transistor, wherein a second transistor is coupled to the first transistor;

reducing the voltage; and

providing the reduced voltage an output of the second transistor, wherein a well, bounding the first transistor and the second transistor, is coupled to the output.

42. The method of claim 41, wherein applying the voltage to the first transistor comprises applying the voltage to a first source/drain and a gate of the first transistor.

43. The method of claim 42, wherein a second source/drain of the first transistor and a first source/drain of the second transistor are integrally formed and are coupled to a gate of the second transistor.

44. The method of claim 43, wherein a second source/drain of the second transistor is coupled to the well and to a semiconductor region containing the source/drains of the first and second transistors.

45. (Amended) A method of reducing voltage, comprising:

applying the voltage to a first transistor, wherein the first transistor is coupled to a second transistor;

reducing the voltage; and

providing the reduced voltage at an output of the second transistor, wherein a first well, bounding the first transistor, is coupled to the second transistor and a second well, bounding the second transistor, is coupled to the output.

46. The method of claim 45, wherein applying the voltage to the first transistor comprises applying the voltage to a first source/drain and a gate of the first transistor.

47. The method of claim 46, wherein a second source/drain of the first transistor is coupled to a first source/drain and a gate of the second transistor and a second source/drain of the second transistor is coupled to the output.

48. The method of claim 47, wherein the well of the first transistor is coupled to the second source/drain of the first transistor and to the first source/drain of the second transistor, and the well of the second transistor is coupled to the second source/drain of the second transistor and to the output.

sub D1 C7

49. (Amended) A method of reducing a voltage, comprising:

applying the voltage to a first source/drain and a gate of a first transistor, wherein a second source/drain of the first transistor is integrally formed with a first source/drain of a second transistor to form a common source/drain and the common source/drain is coupled to a gate of the second transistor;

reducing the voltage; and

providing the reduced voltage at a second source/drain of the second transistor, wherein the voltage is reduced by a threshold voltage of both the first transistor and the second transistor.

50. The method of claim 49, wherein a semiconductor region containing the first and second source/drains and common source/drain of the first and second transistors is coupled to the second source/drain of the second transistor.

51. The method of claim 50, wherein a well bounding the first transistor and the second transistor is coupled to the second source/drain of the second transistor.

52. (Amended) A method of reducing voltage, comprising:

applying the voltage to a first source/drain and a gate of a first transistor, wherein the a second source/drain of the first transistor is coupled to a first source/drain and a gate of a second transistor;

reducing the voltage; and

providing the reduced voltage at a second source/drain of the second transistor, wherein the voltage is reduced by a threshold voltage of both the first transistor and the second transistor.

53. The method of claim 52, wherein a first semiconductor region containing the first and second source/drains of the first transistor is coupled to the second source/drain of the first transistor and wherein a second semiconductor region containing the first and second source/drains of the second transistor is coupled to the second source/drain of the second transistor.

54. The method of claim 53, wherein a first well bounding the first transistor is coupled to the second source/drain of the first transistor and wherein a second well bounding the second transistor is coupled to the second source/drain of the second transistor.

55. A method of regulating a voltage, comprising:

applying the voltage to a voltage reduction circuit; and

applying a signal to a switching circuit coupled to the voltage reduction circuit to cause the voltage reduction circuit to be activated to reduce the voltage by a predetermined amount.

56. The method of claim 55, wherein applying the voltage to the voltage reduction circuit comprises applying the voltage to a first source/drain of a transistor and wherein:

a gate of the transistor is coupled to the switching circuit;

a second source/drain of the transistor is coupled to a node; and

a semiconductor region of the transistor containing the first and second source/drains is coupled to the node.

57. The method of claim 55, further comprising applying the voltage to a second voltage reduction circuit that is coupled to the switching circuit.

58. The method of claim 57, wherein applying the voltage to the second voltage reduction circuit comprises applying the voltage to a first source/drain and a gate of a transistor and wherein a second source/drain of the transistor is coupled to the switching circuit.

59. The method of claim 57, wherein applying the voltage to the second voltage reduction circuit comprises applying the voltage to a first source/drain and a gate of a first transistor, and wherein:

a second source/drain of the first transistor is coupled to a first source/drain and to a gate of a second transistor;

a first well, isolating the first transistor from a substrate, is coupled to the first source/drain of the second transistor;

a second source/drain of the second transistor is coupled to the switching circuit; and

a second well, isolating the second transistor from the substrate, is coupled to the switching circuit.

60. The method of claim 57, wherein coupling another voltage reduction circuit to the switching circuit comprises:

applying the voltage to a first source/drain and a gate of a first transistor, wherein a second source/drain of the first transistor is integrally formed with a first source/drain of a second transistor to form a common source/drain and the common source/drain is coupled to a gate of the second transistor; and

providing a reduced voltage at a second source/drain of the second transistor coupled to the switching circuit, wherein the voltage is reduced by a threshold voltage of both the first transistor and the second transistor.

Sub D1 C9

61. (Amended) A method of regulating a voltage, comprising:

applying the voltage to a first source/drain of a transistor;

reducing the voltage; and

providing the reduced voltage at a second source/drain of the transistor in response to a gate signal applied to a gate of the transistor to activate the transistor.

62. The method of claim 61, further comprising applying the gate signal to the gate of the transistor in response to an enable signal being applied to a switching circuit coupled to the gate.

Sub D1 C10

63. (Amended) The method of claim 62, wherein applying the gate signal to the gate of the transistor comprises:

generating the gate signal by applying the reduced voltage to the switching circuit; and

applying the enable signal to the switching circuit to apply the gate signal to the gate of the transistor.

64. The method of claim 63, wherein generating the gate signal comprises applying the reduced voltage to a voltage divider circuit.

65. (Amended) A method of operating an integrated circuit, comprising:

applying an external voltage to an input of the integrated circuit;

generating a reduced voltage from the external voltage to operate at least one internal circuit of the integrated circuit, wherein generating the reduced voltage includes:

applying the external voltage to a transistor;

reducing the voltage external voltage by a threshold voltage of the transistor; and

providing the reduced voltage at an output of the transistor, wherein the output of the transistor is coupled to a well that isolates the transistor from a substrate of the integrated circuit; and

applying the reduced voltage to the at least one internal circuit.

66. The method of claim 65, wherein applying the voltage to the transistor comprises coupling the external voltage to a first source/drain and a gate of the transistor.

67. The method of claim 66, wherein applying the reduced voltage to the at least one internal circuit comprises coupling a second source/drain of the transistor and a semiconductor region containing the first and second source/drains to the at least one internal circuit.

68. The method of claim 65, wherein the integrated circuit is a memory device and the at least one internal circuit is a memory cell.

Sub D1 C12

69. (Amended) A method of operating an integrated circuit, comprising:

applying an external voltage to an input of the integrated circuit;

generating a reduced voltage from the external voltage to operate at least one internal circuit of the integrated circuit, wherein generating the reduced voltage includes:

applying the external voltage to a source/drain and a gate of a transistor;

reducing the external voltage by a threshold voltage of the transistor; and

providing the reduced voltage at a second source/drain of the transistor, and

applying the reduced voltage to the at least one internal circuit.

70. The method of claim 69, wherein a well that isolates the transistor from a substrate of the integrated circuit is coupled to the at least one internal circuit.

71. The method of claim 69, wherein a semiconductor region containing the first and second source/drain regions is coupled to the at least one internal circuit.

Sub D2 C13

72. (Amended) A method of operating an integrated circuit, comprising:

applying an external voltage to an input of the integrated circuit;

generating a reduced voltage from the external voltage to operate at least one internal circuit of the integrated circuit, wherein generating the reduced voltage includes:

applying the voltage to a first source/drain and a gate of a first transistor, wherein a second source/drain of the first transistor is integrally formed with a first source/drain of a second transistor to form a common source/drain and the common source/drain is coupled to a gate of the second transistor;

reducing the external voltage by a threshold voltage of the transistor by a

C13 rewritten

threshold voltage of both the first transistor and the second transistor; and

providing the reduced voltage at a second source/drain of the second transistor; and

applying the reduced voltage to the at least one internal circuit.

73. The method of claim 72, wherein a semiconductor region containing the first and second source/drains and common source/drain of the first and second transistors is coupled to the at least one internal circuit.

74. The method of claim 73, wherein a well isolating the first and second transistors from a substrate of the integrated circuit is coupled to the at least one internal circuit.

Sub D1

C14

75. (Amended) A method of operating an integrated circuit, comprising:

applying an external voltage to an input of the integrated circuit;

generating a reduced voltage from the external voltage to operate at least one internal circuit of the integrated circuit, wherein generating the reduced voltage includes:

applying the voltage to a first source/drain and a gate of a first transistor, wherein a second source/drain of the first transistor is coupled to a first source/drain and a gate of a second transistor;

reducing the external voltage by a threshold voltage of the transistor by a threshold voltage of both the first transistor and the second transistor; and

providing the reduced voltage at a second source/drain of the second transistor; and

applying the reduced voltage to the at least one internal circuit.

76. The method of claim 75, wherein a first semiconductor region containing the first and second source/drains of the first transistor is coupled to the first source/drain and the gate of the second transistor and wherein a second semiconductor region containing the first and second source/drains of the second transistor is coupled to the at least one internal circuit.

77. The method of claim 75, wherein a first well isolating the first transistor from a substrate of the integrated circuit is coupled to the first source/drain and gate of the second transistor and wherein a second well isolating the second transistor from a substrate of the integrated circuit is coupled to the at least one internal circuit.